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09/872,600	06/01/2001	Kevin B. Leigh	COMP:0213	2616

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EXAMINER	
HUYNH, KIM T	

ART UNIT	PAPER NUMBER
2112	4

DATE MAILED: 01/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/872,600	LEIGH ET AL.	
	Examiner	Art Unit	
	Kim T. Huynh	2112	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-10, 12-21, 23-33, 35-55 are rejected under 35 U.S.C. 102(e) as being anticipated by Yanagisawa (US Patent 6,519,669)

As per claims 1,13, Yanagisawa discloses a method of switching control of a bus in a processor-based device, the method comprising the acts of:

- Electrically coupling a first bus controller to the bus; (col.3, lines 52-58)
- Generating a detection signal indicative of coupling of a second bus controller to the bus; and (col.3, lines 52-67)
- Automatically isolating the first bus controller from the bus in response to the detection signal. (col.3, lines 52-67), wherein disconnecting implies isolating bus controller)

As per claim 2, Yanagisawa discloses the method comprising the act of terminating the first bus controller. (col.3, lines 52-67), wherein detecting control signal, bus switch responding to perform connecting or disconnecting implies terminating)

As per claim 3, Yanagisawa discloses wherein the first bus controller is terminated response to detection of the detection signal. (col.3, lines 52-67)

As per claim 4, Yanagisawa discloses wherein the bus comprises a plurality of traces disposed on a substrate, wherein the first bus controller is electrically coupled to a first segment of the plurality of traces, and wherein the second bus controller is electrically coupled to a second segment of the plurality of traces. (col.3, lines 52-67), (col.5, line 64-col.6, line 12), wherein substrate is equipped with each connector(slots, port, socket)), (col.11, lines 38-60)

As per claim 5, Yanagisawa discloses the method comprising the act of terminating the second segment of the plurality of traces. (col.11, lines 51-60), wherein disable/enable implies terminating)

As per claim 6, Yanagisawa discloses the method comprising the act of electrically removing terminating of the second segment of the plurality of traces in response to detection of the second bus controller. (col.11, lines 51-60)

As per claim 7, Yanagisawa discloses wherein the first bus controller is disposed on a first substrate, and the second controller is disposed on a second substrate, the second substrate being coupled to the first substrate, and wherein the act of generating a detection signal comprises the act of transmitting the detection signal from the second substrate to the first substrate. (col.3, lines 52-67), (col.11, lines 38-60)

As per claim 8, Yanagisawa discloses wherein the first substrate comprises an expansion port, and a first end of the cable is connected to the expansion port. (col.3, lines 22-45)

As per claims 9, 31,50, Yanagisawa discloses wherein the bus comprises a SCSI bus. (col.8, lines 28-38)

As per claim 10, Yanagisawa discloses wherein the first substrate and the second substrate each comprise a printed circuit board. (col.8, lines 39-57), fig.3, 24, wherein cards implies pcb inserted into slot (substrate))

As per claim 12, Yanagisawa discloses wherein the act of electrically coupling comprises the act of coupling the first bus controller to the bus using a switch. (fig.9, 61), (col.3, lines 53-67)

As per claim 14, Yanagisawa discloses wherein the act of detecting the presence of the second bus controller comprises the act of generating a detect signal when the second bus controller is electrically coupled to the bus. (col.3, lines 53-67)

As per claim 15, Yanagisawa discloses wherein the act of automatically switching control of the bus comprises the acts of:

- Isolating the first bus controller from the bus; and (col.3, lines 53-67)
- Terminating the isolated first bus controller. (col.3, lines 53-67)

As per claims 16, 46, Yanagisawa discloses the method comprising the act of terminating the bus proximate the first bus controller. (col.3, lines 53-67)

As per claim 17, Yanagisawa discloses wherein the bus is terminated proximate the first bus controller in response to detecting the presence of the second bus controller. (col.3, lines 53-67)

As per claim 18, Yanagisawa discloses wherein the second bus controller is disposed on a second substrate coupled to the first substrate. (fig.9, 61, wherein bus controller control either 305,307,309 or 311 , one got control the others couple to the controller)

As per claim 19, Yanagisawa discloses wherein the first substrate comprises an expansion port, and the method comprises the act of terminating the bus proximate the expansion port. (col.8, lines 28-38)

As per claim 20, Yanagisawa discloses the method comprising the act of removing termination of the bus proximate expansion port in response to detecting the presence of the second bus controller. (col.3, lines 53-67)

As per claim 21, Yanagisawa discloses the method of switching control of a bus in a low profile server, the low profile server comprising a first bus controller, a bus, and an isolation device, wherein the first bus controller is configured to control the bus, and wherein the isolation device is configured to isolate first bus controller from the bus, the method comprising the act of connecting a second bus controller to the bus to cause the isolation device to isolate the first bus controller from the bus. (col.3, lines 53-67)

As per claims 23, 34, Yanagisawa discloses a processor-based device, comprising:

- A processor; (fig.2, 11)
- A memory coupled to the processor; and (fig.2, 14, 15)
- A first substrate, comprising:
    - A bus disposed on the first substrate; (col.3, lines 53-67)
    - A first bus controller disposed on the first substrate, the first bus controller being coupled to the processor and the bus; and (fig.9)
    - An isolation device disposed on the first substrate, the isolation device being configured to couple the first bus controller to the bus, and to automatically isolate the first bus controller from the bus in response to detection of a second bus controller coupled to the bus. (col.3, lines 53-67), (col.11, lines 32-61)

As per claim 24, Yanagisawa discloses the device comprising an expansion port disposed on the first substrate and coupled to the bus, wherein the expansion port is connectable to a second substrate, and wherein the second bus controller is disposed on the second substrate. (col.8, lines 22-45), (col.5, line 64-col.6, line 12)

As per claim 25, Yanagisawa discloses wherein the second bus controller is disposed on a second substrate, and the device comprises a cable having a first end and a second end, the first end being connectable to the first substrate, and the second end being connectable to the second substrate. (col.5, line 64-col.6, line 12)

As per claim 26, Yanagisawa discloses the device comprising a termination device disposed on the first substrate, the termination device being configured to terminate the bus proximate the expansion port when the second bus controller is not coupled to the bus.(col.3, lines 53-67), wherein disconnecting implies terminating)

As per claim 27, Yanagisawa discloses the device comprising a termination device disposed on the first substrate, the termination device being configured to terminate the bus proximate the first bus controller in response to detection of the second bus controller. (col.3, lines 53-67)

As per claims 28, 39, Yanagisawa discloses wherein the isolation device comprises an electronic switch. (col.3, lines 53-67), fig.9, 61

As per claims 29, 40, Yanagisawa discloses wherein the electronic switch comprises a transistor. (fig.9, 61) wherein transistor in inherently encloses a transistor)

As per claim 30, Yanagisawa discloses wherein the processor and the memory are disposed on the first substrate. (fig.9)

As per claim 32, Yanagisawa discloses the device comprising a SCSI device connectable to the SCSI bus. (col.8, lines 28-45)

As per claims 33,43, Yanagisawa discloses wherein the SCSI device comprises a hard disk drive.(col.8, lines 28-45)

As per claim 36, Yanagisawa discloses the board comprising a termination device disposed on the substrate and configured to terminate the first bus

controller in response to detection of the second bus controller coupled to the bus. (col.3, lines 53-67)

As per claim 37, Yanagisawa discloses the board comprising an expansion port disposed on the substrate and coupled to the bus, wherein the second bus controller is coupled to the bus via the expansion port. (col.3, lines 53-67), (col.11, lines 32-61)

As per claim 38, Yanagisawa discloses the board comprising a termination device disposed on the substrate and configured to terminate the bus proximate the expansion port when the second bus controller is not coupled to the bus via the expansion port. (col.3, lines 53-67)

As per claim 41, Yanagisawa discloses the printed circuited board comprising:

- A memory disposed on the substrate; and (fig.2, 14), wherein memory into slot of board implies disposed on substrate).
- A processor disposed on the substrate, the processor being coupled to the memory and to the first bus controller.(fig.2)

As per claim 42, Yanagisawa discloses wherein a SCSI device is coupled to the bus, the SCSI device being controllable by the first bus controller or the second bus controller. (col.8, lines 28-45)

As per claim 44, Yanagisawa discloses a method of manufacturing a device for switching control of a bus in a processor-based device, the method comprising the acts of:

- Providing a bus disposed on a substrate; (col.3, lines 53-67)

- Connecting an expansion port to the bus, the expansion port being configured for connection to a second bus controller; (col.3, lines 53-67)
- Disposing an isolation device on the substrate, the isolation device being connected to the bus; and (col.3, lines 53-67)
- Disposing a first bus controller on the substrate, the first bus controller being connected the isolation device, the isolation device being configured to isolate the first bus controller from the bus when a second bus controller is connected to the expansion port. (col.3, lines 53-67), (col.11, lines 32-61)

As per claim 45, Yanagisawa discloses the method comprising the act of disposing a termination device on the substrate, the termination device being connected to the bus. (col.3, lines 53-67)

As per claim 47, Yanagisawa discloses the method wherein the termination device is configured to terminate the first bus controller when the second bus controller is connected to the expansion port. (col.3, lines 53-67)

As per claim 48, Yanagisawa discloses wherein the termination device is connected to the bus proximate the expansion port. (col.3, lines 53-67)

As per claim 49, Yanagisawa discloses wherein the termination device is configured to terminate the bus proximate the expansion port when the second bus controller is not connected to the expansion port. (col.3, lines 53-67), (col.11, lines 32-61)

As per claim 51, Yanagisawa discloses wherein the first bus controller comprises a SCSI bus controller. (col.3, lines 28-45)

As per claim 52, Yanagisawa discloses a method of manufacturing an expansion card connectable to system controller board having a system bus controller configured to control the bus, and having an isolation device configured to isolate the system bus controller from the bus in response to a detect signal, the method comprising the acts of:

- Disposing an expansion us controller on a substrate, the expansion bus controller being configured to control a bus; (col.3, lines 53-67)
- Disposing a detect signal generator on the substrate; (col.3, lines 53-67)
- Connecting the detect signal generator to the first expansion connector; and (col.3, lines 53-67)
- Disposing a first expansion connector on the substrate, the first expansion connector connected to the expansion bus controller and the detect signal generator, (col.3, lines 53-67)
- Wherein the first expansion connector is configured to couple with a cable, the cable having a first end connectable to the first expansion connector and a second end connectable to a system controller board, and (col.3, lines 53-67)
- Wherein the detect signal generator is configured to generate a detect signal detectable at the second end of the cable when the expansion

board is connected to the system board via the cable. (col.3, lines 53-67), (col.5, line 64-col.6, line 12)

As per claim 53, Yanagisawa discloses a method of switching between a first device and a second device connectable to a communications medium in a processor-based device, the method comprising the acts of:

- Electrically coupling a first device to the communications medium;(col.3, lines 53-67)
- Generating a detection signal indicative of coupling of a second device to the communications medium; and (col.3, lines 53-67)
- Automatically isolating the first device from the communications medium in response to the detection signal. (col.3, lines 53-67)

As per claim 54, Yanagisawa discloses wherein the communications medium comprises a point-to-point interconnect. (col.3, lines 23-30)

As per claim 55, discloses wherein the communications medium comprises shared bus. (col.1, lines 53-67), wherein acquired ownership of bus implies shared bus)

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 11,22, 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanagisawa (US Patent 6,519,669) in view of Applicant Admitted Prior Art

As per claims 11 and 34, Yanagisawa discloses all the limitations as above except a low profile server. However Applicant admitted prior art discloses designs of low profiles servers which have a reduced height between the base and top of the chassis. (page 2, lines 23-24)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate AAPA's teaching into Yanagisawa's method so as to reduce the height.

As per claim 22, Yanagisawa discloses wherein the first bus controller is disposed on a first substrate, and wherein the second bus controller is disposed on a second substrate, and the act of connecting the second bus controller to the bus comprises the acts of:

- Disposing a cable, the cable comprising a first end and a second end; (col.5, line 64-col.6, line 12)
- Connecting the first end of the cable to the first substrate; and (col.5, line 64-col.6, line 12)
- Connecting the second end of the cable to the second substrate. (col.5, line 64-col.6, line 12)

Yanagisawa discloses all the limitations as above except a low profile server. However Applicant admitted prior art discloses designs of low profiles

servers which have a reduced height between the base and top of the chassis. (page 2, lines 23-24)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate AAPA's teaching into Yanagisawa's method so as to reduce the height.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Chan [USPN 6,633,935] discloses bus termination

Campbell [USPN 6,601,125] discloses traces bus path

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM- 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications and After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

Jan. 21, 2003

Khanh Dang
Primary Examiner